A Review of Electronic Inductor Technique for Power Factor Correction in Three-Phase Adjustable Speed Drives

Davari, Pooya; Yang, Yongheng; Zare, Firuz; Blaabjerg, Frede

Published in:
Proceedings of IEEE Energy Conversion Congress and Exposition (ECCE), 2016

DOI (link to publication from Publisher):
10.1109/ECCE.2016.7854767

Publication date:
2016

Document Version
Publisher's PDF, also known as Version of record

A Review of Electronic Inductor Technique for Power Factor Correction in Three-Phase Adjustable Speed Drives

Pooya Davari†, Yongheng Yang†, Firuz Zare‡, Frede Blaabjerg†

†Department of Energy Technology
Aalborg University, 9220 Aalborg, Denmark
pda@et.aau.dk, yoy@et.aau.dk, fbl@et.aau.dk

‡Power and Energy Group
The University of Queensland, St. Lucia, 4072, Australia
f.zare@uq.edu.au

***Abstract*—Electronic Inductor (EI) techniques are promising approaches for improving the grid-side current quality, and they are suitable for motor drive applications. In this paper, different EI topologies are investigated from the efficiency perspective, including the effect of employing Silicon Carbide (SiC) power devices. Moreover, the influence of partial loading on component sizing in Adjustable Speed Drives (ASDs) is studied. Finally the analytical loss modelling of power switches is utilized for efficiency measurement. The theoretical analyses are verified by experimental benchmarking in an ASD system.**

Keywords—adjustable speed drive; electronic inductor; harmonic elimination; loss estimation; power factor correction

I. INTRODUCTION

Introducing Adjustable Speed Drive (ASD) based on power electronics technology leads to more energy-efficient motor drive systems. Although employing power electronics in ASD systems brings many benefits but it has also made them as one of the major sources of harmonics which may deteriorate the grid power quality and hence lead to high losses and stability issues in the grid [1]-[7].

Fig. 1(a) shows a block diagram of a three-phase motor drive equipped with a diode-rectifier as the first conversion stage following with an intermediate circuit, breaking chopper and finally a voltage source inverter. This unidirectional power flow configuration is the most commonly-employed topology in industrial and commercial drive applications. However, employing three-phase diode rectifiers at the front-end stage imposes a high level of input current harmonics. In order to reduce the generated input current harmonics, passive filtering e.g., using an inductor at the dc-side of the drive as it is shown in Fig. 1(b) is traditionally adopted, being a simple and an effective solution to some extent [2], [4].

The main reasons that in majority of ASD systems a conventional three-phase diode rectifier with passive filter is utilized are due to two main factors. *(A)* Simplicity, high reliability and low-cost of three-phase diode rectifier are the first reason why they are still in use. *(B)* International standards and regulations allow harmonic emissions in ASD systems to have relatively high Total Harmonic Distortion (THD) levels. For example, for a short-circuit ratio of $R_{sce} = 120$ and based on Table 4 in IEC61000-3-12, the THD_i and the fifth current harmonic should be below 48% and 40%, respectively, in the case of higher power levels (16 - 75 A per phase) [8]. Although many high-performance harmonic elimination solutions such as Active Front-End (AFE) rectifiers or Active Shunt Power Filters (ASPF) [2], [6], [10] are available, cost has become the main obstacle for them to expand in the market.

However, the harmonic distortion and its consequences at the grid-side can be elevated when higher numbers of drives are connected to the Point of Common Coupling (PCC). Therefore, it calls for more simple and cost-effective solution to replace the traditional passive filters. Among the prior-art solutions the Electronic Inductor (EI) method [7], [11]-[15] has a great potential to be adopted in three-phase drive systems. The EI is a simple technique which can improve the THD_i and the power factor (λ) independent of the load profile. More importantly, it can be added as an intermediate circuit as shown in Fig. 1(c)-(e), and hence no major modification is needed on the conventional ASD systems.

The main goal of this paper is to analyze the existing EI topologies operating in the Continuous Conduction Mode (CCM) with respect to efficiency and their cost and stability potential to be adopted in ASD systems. Moreover, the effect of the partial loading condition on proper component sizing in ASDs has been addressed and advantages of employing SiC power devices in boost topologies have been considered. Finally, the theoretical analysis is validated through experimental benchmarking in a motor drive system.

II. CONVENTIONAL THREE-PHASE DIODE RECTIFIER

In this section, the behavior of the widely-used three-phase diode rectifier with a passive filter at the dc-side (Fig. 1(b)) is discussed. Generally, the passive filtering solution has two major drawbacks. First, in order to obtain the maximum performance (i.e., $THD_i \approx 30\%$ and $\lambda \approx 0.95$), it requires a large inductor. Fig. 2(a) illustrates input current waveforms (i.e., i_a) at different inductor values following Fig. 1(b) at the rated output power based on the system parameters given in Table I and II.

As can be seen, only for large inductor values, the THD_i and λ can be improved (Fig. 2(a)). In practice the inductance value is selected in the range of 3-5% (i.e., 2mH < L_{dc} < 3.5mH), which can be calculated as,

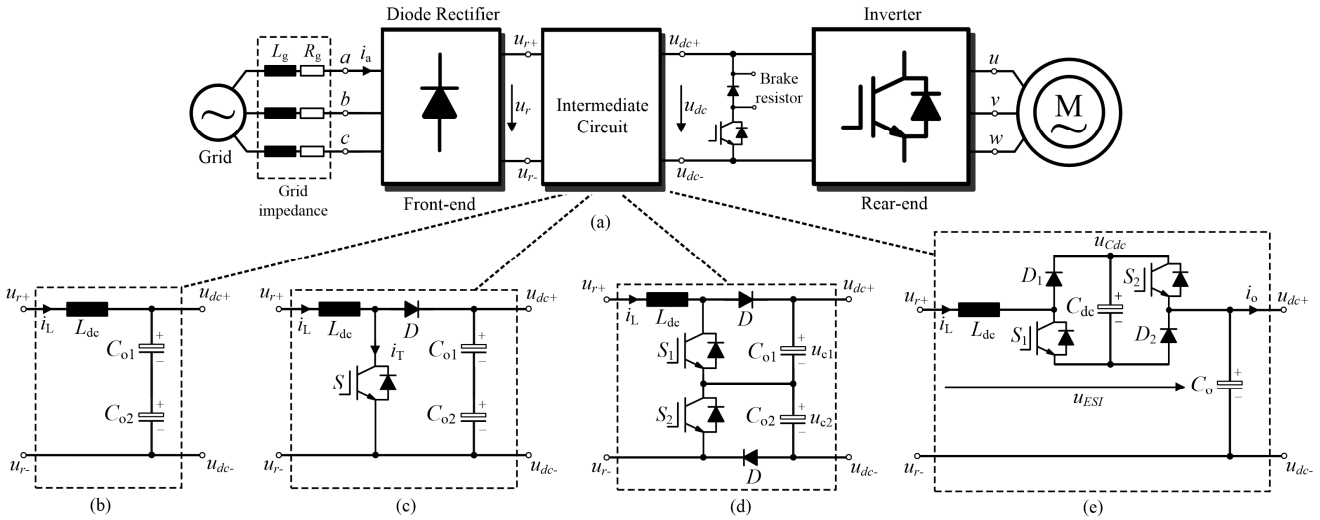

Fig. 1: A block diagram of a standard ASD system showing (a) double stage conversion (unidirectional) using different intermediate circuits at dc-side with (b) passive filtering, (c) single-switch boost converter, (d) double-switch boost converter, (e) electronic smoothing inductor.

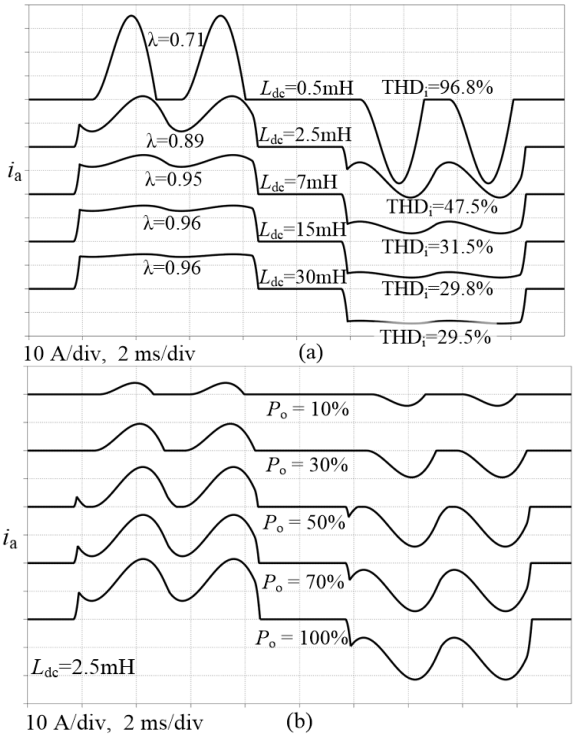

Fig. 2: Simulated input current waveform (i_a) in a three-phase diode rectifier using dc-side passive filtering: (a) effect of dc-link inductor size, (b) effect of loading condition following Table I&II.

$$Z_L(\%) = \frac{X_L \hat{I}_{(1)}}{\hat{U}_N} \qquad (1)$$

where X_L is the inductor impedance at grid frequency, $\hat{I}_{(1)}$ is the peak amplitude of grid fundamental current and $\hat{U}_N$ is the peak amplitude of the grid phase voltage.

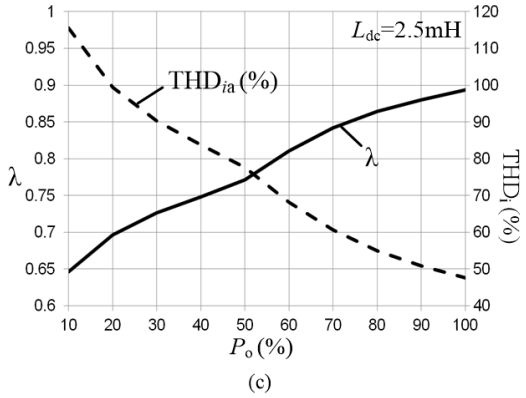

Fig. 3: Numerical simulation of a three-phase diode rectifier using dc-side passive filtering showing corresponding power factor λ and input current THD of the input current waveform (i_a) at different output power levels following Table I&II.

TABLE I. PARAMETERS OF THE SYSTEM (Fig. 1(a))

Symbol	Parameter	Value
$U_{g,LL,rms}$	RMS line-to-line voltage of the grid	400 Vrms
f_g	Grid frequency	50 Hz
L_g, R_g	Grid Impedance	0.18 mH, 0.1 Ω
$P_{o,max}$	Rated power (P_o = 100%)	7.5 kW

According to (1), the second shortcoming is the effective impedance of the passive filter at the fundamental frequency (f_g) which is proportional to the load current. Fig. 2(b) and Fig. 3 illustrate the input current waveforms as well as the THD_i and power factor (λ) performance under different output power loading conditions. It can be observed that the THD_i and λ will be worsened when the rectifier is partially loaded. In fact, this

TABLE II. EMPLOYED SYSTEM PARAMETERS IN EACH TOPOLOGY (FIG. 1(b)-(e))

Topology	f_{sw} (kHz)	$f_{sw,eff}$ (kHz)	L_{dc0} (mH)	U_{dc} (V)	C_{o1}= C_{o2} (mF)	C_{dc} (mF)	C_o (mF)
Passive Filter (Fig. 1(b))	--	--	2.5	540	1	--	--
Single-Switch Boost (Fig. 1(c))	35	35	2	700	1	--	--
Three-Level Boost (Fig. 1(d))	35	70	0.68	700	1	--	--
ESI (Fig. 1(e))	35	70	0.2	540	--	1.5	0.047

is an important issue as a majority of ASD applications operate in partial loading conditions.

III. ELECTRONIC INDUCTOR TECHNIQUE

As it is already mentioned, having a large inductor at the dc-side can improve the THD_i and λ. However, a large inductor substantially impairs the power density, efficiency, cost and dynamic behavior of the system. The basic idea of the EI is to replace the bulky dc-side inductor with a relatively small inductor incorporated by a dc-dc converter which can emulate an electrical behavior of an ideal infinite inductor [7], [11]-[15]. In this situation, the input current at the grid side (i.e., $i_{a,b,c}$) will be a square-wave with 120 degrees conduction, resulting in $THD_i \approx 30\%$ and $\lambda \approx 0.95$ (under a balanced grid condition).

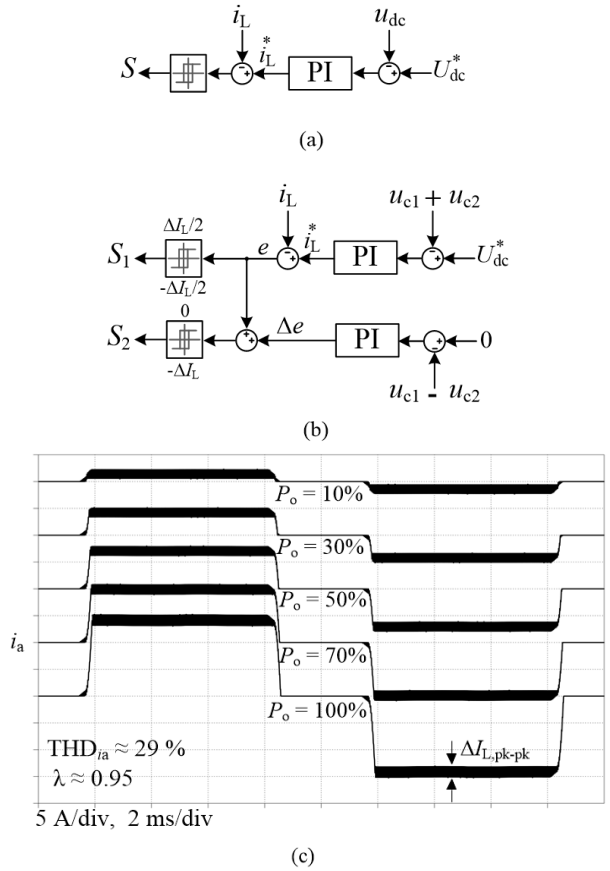

Fig. 4: Boost converter topology: (a) control structure for the single-switch topology in Fig. 1(c), (b) control structure for the three-level boost in Fig. 1(d), and (c) simulated input current waveforms at different power levels following Table I&II.

A. Boost Converter-based EI

The simple approach to realize an EI is to locate a boost converter in cascade with the diode rectifier at the dc side (Fig. 1(c)). The main advantage of such topology lies in its simplicity in control, as shown in Fig. 4(a), and its ability to boost the output voltage. In this topology, the voltage stress across the power switch is equal to the output dc-link voltage (i.e., 700 V). An alternative topology known as three-level boost converter [11] is shown in Fig. 1(d), and by employing a three-level control approach (Fig. 4(b)) it increases the effective switching of the inductor current by a factor of two. Therefore, it is an important size reduction factor for the boost inductor as it is shown in Table II. This topology results in halving the voltage stress across the power switches. In both topologies, the dc-link inductor current (i_L) is controlled in CCM at a constant level, and therefore the grid currents will be rectangular as shown in Fig. 4(c). Assuming that the switching frequency f_{sw} is high, the inductance value and the switching frequency can be calculated as follows,

$$L_{dc0} = \frac{U_{dc} D(1-D)}{f_{sw,eff} \Delta I_{L,pk-pk}},$$

$$where \begin{cases} f_{sw,eff} = f_{sw} = \dfrac{D(1-D)U_{dc}}{L_{dc0}\Delta I_{L,pk-pk}} & conventional \quad boost \\ f_{sw,eff} = 2f_{sw} = \dfrac{2D(0.5-D)U_{dc}}{L_{dc0}\Delta I_{L,pk-pk}} & three-level \quad boost \end{cases} \quad (2)$$

where U_{dc} is the average value of the output voltage, $f_{sw,eff}$ is the effective switching frequency of the inductor current, f_{sw} is the switching frequency of the power device, $\Delta I_{L,pk\text{-}pk}$ is the peak-to-peak inductor current ripple, and D is the steady-state duty cycle of the boost converter. Here, L_{dc0} is the unbiased initial inductance. Thereby, the effect of the biased inductor at different current levels needs to be considered as it is addressed in the next section.

Therefore, according to (2) with the applied situation (see, Table I and II), the inductor value in the three-level topology is approximately three times lower than the one in the single-switch topology. Notably, for both cases the ripple factor which is defined in (3) has the same value.

$$k_{ripple}(\%) = 100 \times \frac{0.5\Delta I_{L,pk-pk}}{I_L} \quad (3)$$

In order to extend the CCM operation over a wide range of the loading profile (e.g., 10% to 100%), the minimum required inductance value should be calculated based on the maximum possible $f_{sw,eff}$ and the minimum loading condition ($P_{o,min}$)

considering the Boundary Conduction Mode (BCM). Therefore, rearranging (2) yields,

$$L_{dc0} > \frac{D(1-D)^2 U_{dc}^2}{2P_{o,\min} f_{sw,eff}} \tag{4}$$

Fig. 4(c) illustrates the simulated input current waveforms at various loading conditions using the parameters in Table I and II. As it can be seen, the input current THD and λ have become independent of the loading conditions, which is in contrast to the passive filtering method (e.g., Fig. 2 (b) and Fig. 3). Notably, here using hysteresis current control will not result in a significant-dispersed frequency spectrum as the input voltage (U_r) is a rectified voltage with a small ripple [15].

B. Electronic Smoothing Inductor (ESI)

Another alternative to imitate the behavior of a large inductor is presented in [13], [14]. This topology as shown in Fig. 1(e) employs an asymmetric H-bridge inverter with a small inductor in series with the diode rectifier. Basically, the ESI is a current source which smooths the dc-link current (same functionality as the boost topology). Here, the ESI follows the same principle as the series active filtering by generating the same ripple voltage appearing in the rectified voltage and consequently making the output voltage across C_o equal to the average rectified voltage ($U_{dc} = U_r$). Ideally, the ESI voltage u_{ESI} varies within [13]

$$-0.093U_r < u_{ESI} < 0.047U_r \tag{5}$$

Fig. 5(a) illustrates a three-level control (i.e., $f_{sw,eff} = 2f_{sw}$) applied to the ESI based on inclusion of i_o which acts as a feedforward. Notably, the cut-off frequency (f_c) of the Low Pass Filter (LPF_1) is selected at 5 kHz which removes the effect of switching frequency and pulsating currents from i_o. The cut-off frequency of LPF_2 is selected at 400 Hz which smooths the applied duty cycle and finally the high-pass filter (f_c = 700Hz) is used to block the low frequency components of the rectifier current [13]. To control the voltage across the floating capacitor C_{dc} an offset (Δd) should be added to the duty cycle. The main advantage of this topology is its ability to maintain a low voltage across C_{dc}. This makes it more cost-effective as low voltage power switches for which fast switching performance can be adopted. Moreover, it results in very low power dissipation (see Section V). Considering the BCM operation the minimum initial inductance L_{dc0} based on $P_{o,min}$ is give as,

$$L_{dc0} > \frac{U_{dc}U_{Cdc}D_{max}}{2f_{sw,eff}P_{o,min}} \quad where \quad D_{max} = \frac{1}{4} \tag{6}$$

Fig. 5(b) shows the obtained input current waveforms with the conditions in Table I and II. Here, considering (3) U_{Cdc} is selected as 70 V ($U_{Cdc} \approx 0.12U_r$). Although this topology is compact and has good performance but to be able to control the voltage across the floating capacitor and prevent from the high voltage during the startup, the capacitor (C_{dc}) should be selected quite large compared with C_o (Table II). Secondly, since it requires relatively small inductance, its performance significantly depends on the grid impedance. Finally, it cannot boost the output voltage same as a boost topology.

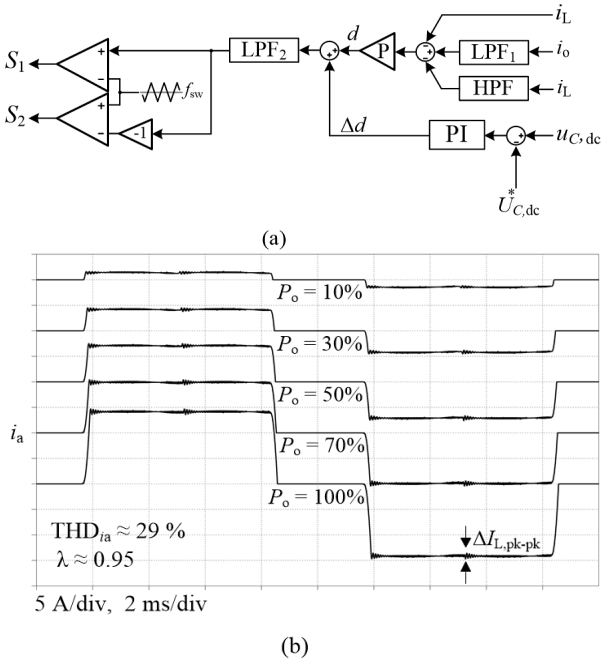

Fig. 5: ESI topology: (a) control structure, (b) simulated input current waveforms at different power levels following Table I & II.

IV. Loss Modeling

Loss modeling of a power electronics system with fast switching transients is not a trivial task. Even with a precise modelling, the presence of the parasitic components in practice makes the estimated loss slightly different from the practical one. In this section the loss modeling is briefly explained based on an analytical approach. Since the aim is to compare different electronic inductor topologies, only the losses at the front-end stage are considered and the inverter and EMI filter losses have been excluded.

The bridge rectifier total losses P_{bridge} can be modeled as,

$$P_{bridge} = 6 \times \left(V_{fb} \frac{I_L}{3} + r_{fb} \frac{i^2_{a,rms}}{\sqrt{2}} \right) \tag{7}$$

where V_{fb} and r_{fb} are the forward voltage and on-state resistance of each diode, respectively. The power switch losses can be given by its conduction losses $P_{T,cond}$ and its switching losses $P_{T,sw}$ as,

$$P_{T,cond} = V_{ce} I_T + r_{Ton} i^2_{T,rms} \quad , \quad P_{T,sw} = \left(E_{on} + E_{off} \right) f_{sw} \tag{8}$$

with I_T and $i_{T,rms}$ being the average and the RMS current flowing through the power switch and r_{Ton} is the on-state resistance. Notably, V_{ce} is only presented in the case of Silicon (Si) power switch (i.e., IGBT). E_{on} and E_{off} are the turn-on and the turn-off energy and should be extracted from the device datasheet and re-scaled to the converter operating conditions. The boost diode conduction $P_{D,cond}$ and the switching $P_{D,sw}$ losses can be estimated as,

$$P_{D,cond} = V_{fo} I_D + r_{fo} i^2_{D,rms} \quad , \quad P_{D,sw} = \begin{cases} E_{rr} f_{sw} & Si \\ Q_c U_{dc} f_{sw} & SiC \end{cases} \tag{9}$$

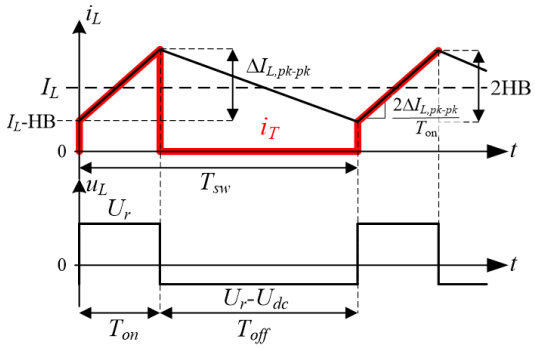

Fig. 6: Typical inductor and power switch current waveforms during one switching cycle in the CCM operation following Fig. 1(c).

in which V_{fo} and r_{fo} are the forward voltage and on-state resistance of the diode. Notably, in the case of the SiC diode there is almost no reverse recovery loss however the effect of the diode junction charge Q_C should be considered. It is to be noted that all current and voltage values can be extracted based on analytical calculations. The advantage of using analytical method is its less computational burden comparing with the numerical simulations. In order to exemplify this, the current and voltage waveforms in a single-switch boost converter operating in CCM is illustrated in Fig. 6. Following the power switch current waveform (e.g., i_T in Fig. 1(c)) the RMS value of this current can be calculated as

$$\begin{aligned} i_{T,rms} &= \sqrt{\frac{1}{T_{sw}}\int_0^{T_{on}}\left(\frac{2\Delta I_{L,pk-pk}}{T_{on}}t + \left(I_L - \Delta I_{L,pk-pk}\right)\right)^2 dt} \\ &= \sqrt{D\left(I_L^2 + \frac{\Delta I_{L,pk-pk}^2}{3}\right)} \end{aligned} \tag{10}$$

Notably, in order to increase the accuracy the above calculation should be averaged over a one grid period.

The switching losses can be finalized by including the gate driver loss P_{gate} as a small portion of the switching losses. This can be done for all three types of switches as,

$$P_{gate} = Q_G(V_{Gon} - V_{Goff})f_{sw} \tag{11}$$

where Q_G is the gate charge and V_{Gon} and V_{Goff} are the gate turn-on and turn-off voltages. Notably, the losses in (8)-(9) and (11) should be multiplied with the number of the components in each topology.

The next step is to calculate the inductor losses which can be separated into copper losses P_{cu} and core losses P_{core}. The copper losses comprise of resistive losses $P_{cu,dc}$ due to the winding resistance and eddy-current losses $P_{cu,edd}$ due to skin and proximity effects given by,

$$P_{cu} = P_{cu,dc} + P_{cu,edd} \qquad where \qquad \begin{cases} P_{cu,dc} = {I_L}^2 R_{Ldc} \\ P_{cu,edd} = {i_{Lac,rms}}^2 R_{Lac} \end{cases} \tag{12}$$

where $i_{Lac,rms}$ is the inductor current ripple and the R_{Lac} is the resistance of the windings at the effective switching frequency. Here, in order to calculate R_{Ldc} and R_{Lac} an impedance analyzer has been used. As can be seen, increasing the current ripple (ΔI_L) can significantly increase the eddy-current loss. The most important equation to determine the core losses P_{core} is the Steinmetz equation,

$$P_{core,v} = k\left(B_{pk}\right)^a \left(f_{sw,eff}\right)^b \tag{13}$$

in which $P_{core,v}$ is the time-average power loss per unit volume and the parameters k, a, and b can be found in the datasheets [19]. However, the above equation is only valid for sinusoidal current waveforms, therefore in order to obtain a good estimation, as it is discussed in [16], the core losses P_{core} is calculated following improved Generalized Steinmetz Equation (iGSE) [17],

$$P_{core,v} = \frac{1}{T}\int_0^T k_i \left|\frac{dB}{dt}\right|^b (\Delta B)^{a-b}\, dt \tag{14}$$

$$k_i = \frac{k}{(2\pi)^{b-1}\int_0^{2\pi}\left|\cos\theta\right|^b 2^{a-b}\, d\theta} \tag{15}$$

The above equation can be simplified as [18]

$$P_{core,v} = k_i f_{sw,eff} \Delta B^{a-b} \sum_j \left(\frac{U_{Ldc,j}}{NA_e}\right)^b \Delta t_j \tag{16}$$

$$k_i = \frac{k}{2^{a+1}\pi^{b-1}\left(0.2761 + \frac{1.7061}{b+1.354}\right)} \tag{17}$$

here N stands for the number of the turns, $U_{Ldc,j}$ is the voltage across the dc-link inductor during the switching time interval of Δt_j. Eventually the inductor core loss P_{core} can be calculated as

$$P_{core} = l_e A_e N_c P_{core,v} \tag{18}$$

where l_e is the effective magnetic path length, A_e is the effective cross section area and N_c is the number of the stacked cores. (16)-(18) can give a good power loss estimation while the converter operates in a CCM. Notably, the core eddy losses have been neglected in this analysis.

It should be noted that, depending on the output power (i.e., I_L) and the type of the core, the inductor permeability may drop with respect to the power and frequency levels, which reduces the inductance value. Therefore, in order to have the calculated inductance at the intended power, the inductance value should be selected slightly larger than the estimated one. Otherwise, in order to maintain the ripple current at the calculated value, the switching frequency should be increased. The ratio of the effective permeability μ_{eff} to the initial permeability μ_i can be estimated as below (the stated parameters can be found in the selected core datasheet [19]),

$$L_{dc} = \left(\frac{\mu_{eff}}{\mu_i}\right) L_{dc0} = \left(c + dH + eH^2 + fH^3 + gH^4\right) L_{dc0} \tag{19}$$

The effect of the inductance drop at different loading conditions has been considered for the simulated waveforms shown in Fig. 4(c) and Fig. 5(b) and in all comparative results

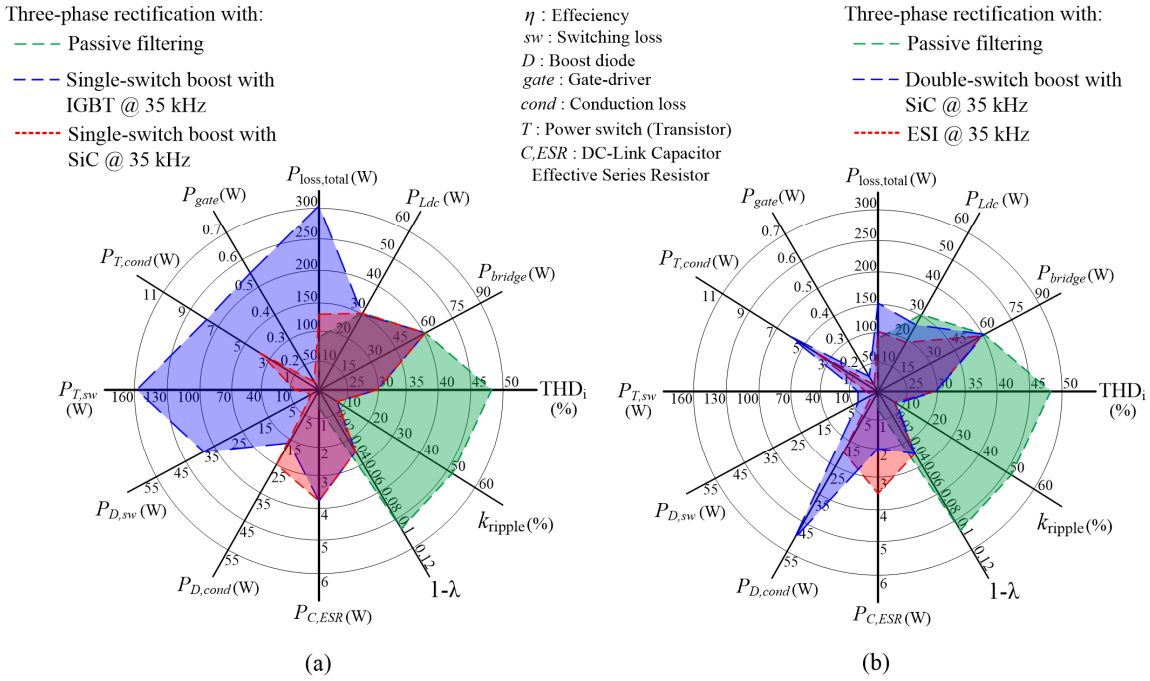

Fig. 7: Comparative results based on the loss modeling of different intermediate circuits in comparison with passive filtering: (a) efficiency performance of single-switch boost topology using Si-IGBT module [SK60GAL125] and SiC MOSFET [C2M0080120D] with SiC diode [C4D15120A], (b) efficiency performance of double-switch boost topology using SiC MOSFETs [C2M0080120D] with SiC diodes [C4D15120A] and ESI using OptiMOS MOSFETs [BSB165N15NZ3] with Si Schottky diodes [APT15S20K] (For all three active methods the dc-link inductor is a XFlux 60µ inductor (55906A2) [19], for IGBT the gate resistance (R_g) is equal to 30 Ω and for the other power devices R_g = 2.5 Ω).

in the next section. Finally the output capacitor losses should be considered based on its Effective Series Resistance (ESR), which is a frequency dependent parameter. Thereby, in order to calculate the capacitor losses, the ESR needs to be extracted based on the spectral component of the capacitor current [20],

$$P_{Co} = \sum_{f} r_{ESR}(f) i^2_{Co,rms}(f) \qquad (20)$$

This value can be found in the datasheet, but in order to estimate the loss accurately the ESR needs to be extracted using an impedance analyzer. However, the loss calculation for the output capacitor is even more complex. For instance as an electrolytic capacitor is normally used, due to its low self-resonant frequency and high capacitance/volume, it is a common practice to connect high frequency capacitors in order to filter high frequency noises. Thus, to be able to accurately calculate the output capacitors losses, the impedance responses of the parallel capacitors need to be extracted individually to be able to estimate the current distribution between them at different frequencies. As it is shown in the next section, the experimental and analytical results have a close agreement which shows the effectiveness of the applied analytical modelling approach.

V. Results

In this section, firstly, the analytical modeling is applied to compare and investigate the efficiency of all topologies shown in Fig. 1(b)-(e). Secondly, the performance and efficiency of a single-switch boost topology is experimentally verified.

Notably, all the parameters both in the theoretical and the experimental analyses are utilized as in Table I and II.

Fig. 7 compares the efficiency of all presented topologies at the rated output power of 7.5 kW. Although the passive filtering method does not show a better performance compared to the EI technique in terms of THD_i and λ, as it can be seen from Fig. 7, it has a high efficiency with total power losses of 91.6 W (η = 98.8%). In order to highlight the effect of using SiC power devices to improve the efficiency of the EI, loss calculation of the single-switch boost topology in Fig. 1(c) is

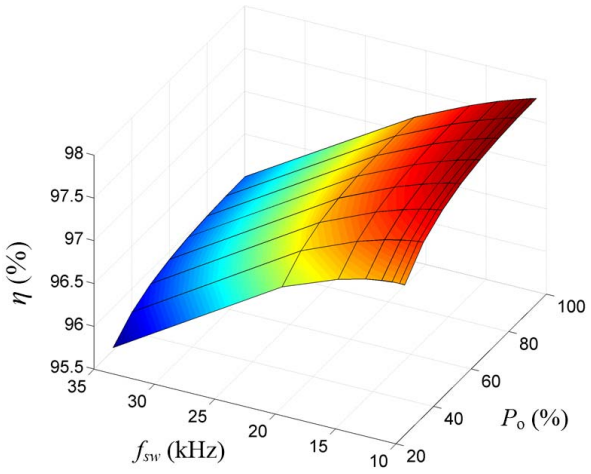

Fig. 8: Dependency of the system efficiency on the utilized switching frequency and output power level in a single-switch boost converter using an IGBT power switch.

also considered with a Si-based power switch Insulated Gate Bipolar Transistor (IGBT). Fig. 7(a) shows a total power loss of 315 W (η = 96%) while using SiC power devices, the loss is significantly reduced down to 131.5 W (η = 98.3%). The obtained results clearly show the high contribution of the switching losses in the IGBT-based system. This is contrary to the SiC-based system, where its only disadvantage is due to the higher SiC diode conduction loss.

Fig. 7(b) shows the loss comparison of a double-switch boost converter with SiC power switches and ESI topology versus the passive filtering technique. As it can be seen, the high conduction losses of the two boost diodes in the double-switch boost converter topology of Fig. 1(d) reduces the system efficiency even though it has a smaller inductor. Compared with a SiC-based single-switch boost converter, the double-switch boost converter has lower efficiency (154.5 W). Thereby, the higher number of the power switches and required voltage sensors in addition to its lower efficiency makes this topology not a suitable choice for an EI system.

In contrast, the ESI topology can attain a substantially high efficiency due to low voltage requirement of the asymmetric H-bridge using the floating capacitor. Also possibility of using low voltage Si Schottky diodes (having lower conduction losses) further improves the energy saving in this topology. As Fig. 7(b) shows, the ESI topology achieved the total power loss of 102.5 W (η = 98.65%) which makes it the only topology with comparable losses comparing with the passive filtering method. Notably, here the number of the stacked cores (i.e., N_c) for single-switch, double-switch and ESI topologies is three, two and one respectively. This shows smaller physical size of the inductor in double-switch boost converter and ESI comparing with the single-switch boost topology due to their higher effective switching frequency.

The losses in a power electronic converter are highly dependent on the applied switching frequency and output power levels. Fig. 8 shows this dependency in the IGBT-based single-switch boost topology at different output power levels and switching frequencies. This curve shows two important trends. First, the highest efficiency can be obtained at higher output power levels. This is due to the lower core losses in the inductor as the current ripple is lower at higher output power. Secondly, the system efficiency can be optimized by applying a suitable switching frequency depending on the output power level.

In order to verify the performed analytical analysis, experimental tests have been conducted on a 7.5 kW three-

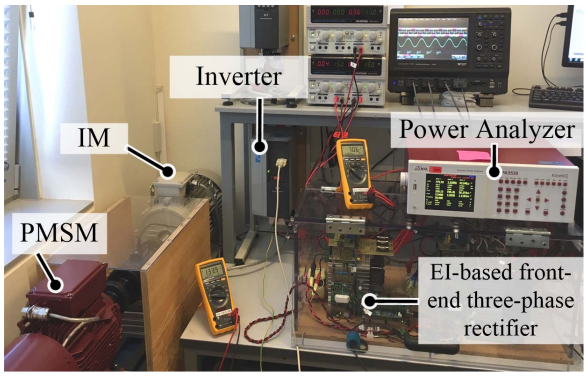

Fig. 9: Experimental test bench of an EI-based front-end three-phase rectifier in a motor drive system with an Induction Motor (IM) coupled with a Permanent Magnet Synchronous Motor (PMSM) as a load.

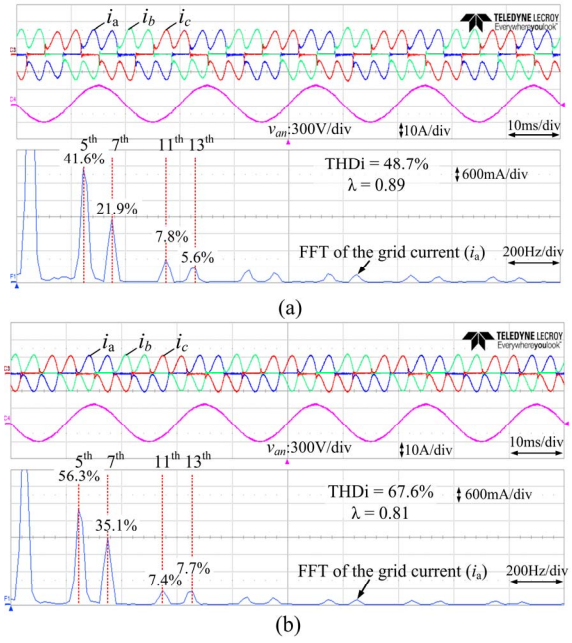

Fig. 10: Experimental measurements of three-phase input current waveforms and its harmonic distribution in a motor drive system with passive filtering technique (dc-side inductor) at partial loadings: (a) measured waveforms at T_m = 35 Nm and 5 kW, (b) measured waveforms at T_m = 28 Nm and 3 kW.

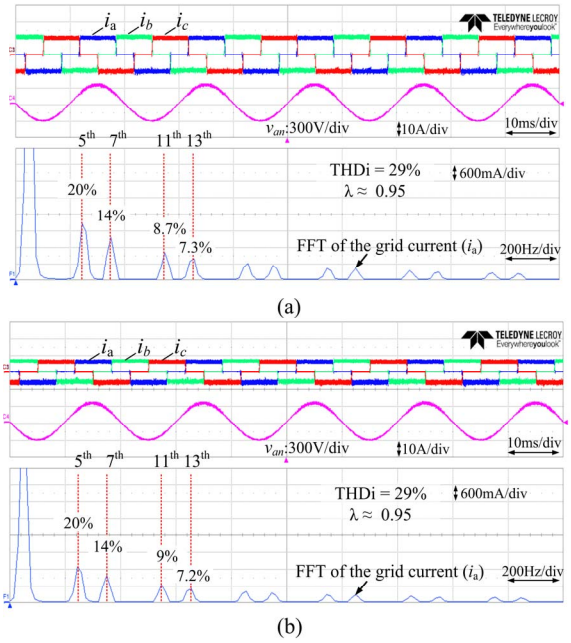

Fig. 11: Experimental measurements of three-phase input current waveforms and its harmonic distribution in a motor drive system with EI technique (IGBT-based single-switch boost) at partial loadings with f_{sw} = 35 kHz and U_{dc} = 700 V: (a) measured waveforms at T_m = 35 Nm and 5 kW, (b) measured waveforms at T_m = 28 Nm and 3 kW.

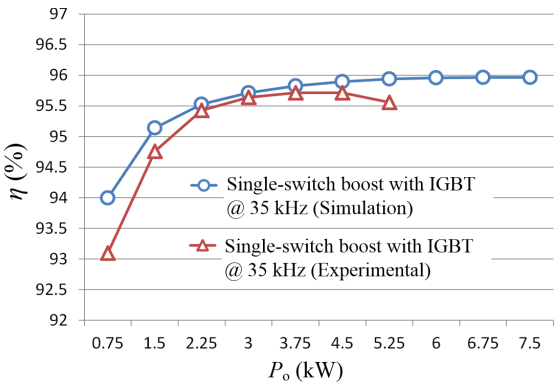

Fig. 12: Experimental efficiency measurement and analytical loss modeling in an IGBT-based single-switch boost topology.

phase motor drive system equipped with an EI (IGBT-based single-switch boost), as it is shown in Fig. 9. Firstly, to highlight the influence of the EI technique, the performance of a motor drive system with and without applying the EI technique is presented in Fig. 11 and Fig. 12. The obtained results in Fig. 10 clearly show that under partial loadings condition with the conventional passive filtering the THD_i and λ are adversely affected. This completely follows the simulated results shown in Fig. 2 and Fig. 3. On the other hand, Fig. 11 shows the input current waveforms at the same power levels as in Fig. 10 when the EI technique is applied. As it can be seen, under partial loading conditions the THD_i and λ are kept equal to 29% and 0.95 respectively.

Finally, Fig. 12 shows the measured experimental efficiency versus the analytical analysis when the output power level is changed from 10% to 100%. As it can be seen, the obtained results are in a close agreement with the preformed analytical loss modelling. This also validates the trend of having a better efficiency at higher power as shown in Fig. 8 due to lower inductor core losses.

VI. Conclusions

In this paper, the performances of different EI techniques utilized in three-phase ASD systems have been investigated. More attention has been given to the efficiency performance of these techniques with and without Wide Band-Gap (WBG) switching devices since it is one of the important factors in the market competition. Load independence performance of the EI techniques has been analyzed in the partial loading condition which is an important issue in conventional drives with passive filtering methods. Control methods and loss modeling approach have been investigated for each EI topology with its own unique capabilities which can be adopted in ASD applications. For instance, the ESI has very low power losses but it requires more sensors, power switches and it does not have boost capability. On the other hand, the boost topology using SiC devices in addition to small power losses has simple control structure and can step-up the DC-link voltage. However, the SiC-based boost system is costly at present. Experimental tests along with more comprehensive analysis have been included in order to verify the proposed analysis.

References

[1] P. Sutherland and B. Brusso, “History of Harmonics”, *IEEE Ind. Appl. Mag.*, vol. 21, no. 3, pp. 6-11, 2015.

[2] J. W. Kolar and T. Friedli, “The essence of three-phase PFC rectifier systems: Part I,” *IEEE Trans. Power Electron*., vol. 28, no. 1, pp. 176–198, Jan. 2013.

[3] J.W. Gray and F. J. Haydock, "Industrial power quality considerations when installing adjustable speed drive systems," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 646-652, May/Jun 1996.

[4] D. Kumar and F. Zare, “Harmonic analysis of grid connected power electronic systems in low voltage distribution networks,” *IEEE J. Emerg. Sel. Top. Power Electron*., vol. 4, no. 1, pp. 70-79, Jan. 2016.

[5] Danfoss: *Facts worth knowing about frequency converters*, Danfoss, Nordborg, Denmark, 2008.

[6] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of three-phase improved power quality AC-DC converters," *IEEE Trans. Ind. Electron.,* vol. 51, pp. 641-660, 2004.

[7] P. Davari, Y. Yang, F. Zare, and F. Blaabjerg, “Predictive pulse pattern current modulation scheme for harmonic reduction in three-phase multi-drive systems”, *IEEE Trans. Ind. Electron,* in press, 2016.

[8] *Electromagnetic compatibility (EMC) - Part 3-12: Limits - Limits for harmonic currents* produced *by equipment connected to public low-voltage systems with input current >16 A and ≤ 75 A per phase, IEC 61000-3-12, 2004.*

[9] M. M. Swamy, “An electronically isolated 12-pulse autotransformer rectification scheme to improve input power factor and lower harmonic distortion in variable-frequency drives,” *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 3986–3994, Sept 2015.

[10] H. Akagi, "Modern active filters and traditional passive filter," *Bulletin of the polish academy of sciences technical sciences*, vol. 54, 2006.

[11] Y. Yang, P. Davari, F. Zare, and F. Blaabjerg, "A dc-link modulation scheme with phase-shifted current control for harmonic cancellation in multi-drive applications," *IEEE Trans. Power Electron.*, vol. 31, no. 3, pp. 1837-1840, Mar. 2016.

[12] C. Klumpner, F. Blaabjerg, and P. Thogersen, "Alternate ASDs: evaluation of the converter topologies suited for integrated motor drives," *IEEE Ind. Appl. Mag.*, vol. 2, no. 2, pp. 71-83, 2006.

[13] H. Ertl and J. W. Kolar, "A constant output current three-phase diode bridge rectifier employing a novel "Electronic Smoothing Inductor", *IEEE Trans. Ind. Electron.*, vol. 52, pp. 454-461, 2005.

[14] J. Salmon and D. Koval, "Improving the operation of 3-phase diode rectifiers using an asymmetrical half-bridge DC-link active filter," *in Proc. of industry Applications Conference,* 2000, pp. 2115-2122, vol.4.

[15] P. Davari, F. Zare, and F. Blaabjerg, “Pulse pattern modulated strategy for harmonic current components reduction in three-phase AC-DC converters”, *IEEE Trans. Ind. Appl.*, vol. pp, no. 99, pp. 1-11, in press, July/Aug 2016.

[16] J. Muhlethaler, J. Biela, J. W. Kolar and A. Ecklebe, "Improved Core-Loss Calculation for Magnetic Components Employed in Power Electronic Systems," *IEEE Trans. Power Electron*, vol. 27, no. 2, pp. 964-973, Feb. 2012.

[17] J. Reinert, A. Brockmeyer, and R. De Doncker, “Calculation of losses in ferro- and ferrimagnetic materials based on the modified Steinmetz equation,” *IEEE Trans. Ind. Appl.*, vol. 37, no. 4, pp. 1055–1061, Jul./Aug. 2001.

[18] T. Nussbaumer, K. Raggl and J. W. Kolar, "Design Guidelines for Interleaved Single-Phase Boost PFC Circuits," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2559-2573, July 2009.

[19] “Magnetics,” Powder Cores Catalog, 2015. [Online]. Available: www.mag-inc.com.

[20] J. W. Kolar and S. D. Round, "Analytical calculation of the RMS current stress on the DC-link capacitor of voltage-PWM converter systems," in *IEE Proceedings - Electric Power Applications*, vol. 153, no. 4, pp. 535-543, July 2006.